

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance outputs when $V_{CC} = 0$ V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74LVC373A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay	$C_L = 50$ pF; $V_{CC} = 3.3$ V		
	Dn to Qn		3.0	ns
	LE to Qn		3.1	ns
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per latch	$V_{CC} = 3.3$ V; notes 1 and 2	14	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. The condition is $V_I = \text{GND to } V_{CC}$.

The 74LVC373A is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state outputs for bus-oriented applications. A latch enable input (pin LE) and an output enable input (pin \overline{OE}) are common to all internal latches.

The 74LVC373A consists of eight D-type transparent latches with 3-state true outputs. When pin LE is HIGH, data at the D-inputs (pins D0 to D7) enters the latches. In this condition, the latches are transparent, i.e. a latch output will change each time its corresponding D-input changes. When pin LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of pin LE. When pin \overline{OE} is LOW, the contents of the eight latches are available at the Q-outputs (pins Q0 to Q7). When pin \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of input pin \overline{OE} does not affect the state of the latches.

The 74LVC373A is functionally identical to the 74LVC573A, but the 74LVC573A has a different pin arrangement.

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT			INTERNAL LATCHES	OUTPUT
	\overline{OE}	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	X	X	X	Z

Note

- H = HIGH voltage level;
h = HIGH voltage level one setup time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one setup time prior to the HIGH-to-LOW LE transition;
X = don't care;
Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC373AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC373ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC373APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC373ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	\overline{OE}	output enable input (active LOW)
2	Q0	latch output
3	D0	data input
4	D1	data input
5	Q1	latch output
6	Q2	latch output
7	D2	data input
8	D3	data input
9	Q3	latch output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	LE	latch enable input (active HIGH)
12	Q4	latch output
13	D4	data input
14	D5	data input
15	Q5	latch output
16	Q6	latch output
17	D6	data input
18	D7	data input
19	Q7	latch output
20	V _{CC}	supply voltage

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V _I	input voltage		0	5.5	V
V _O	output voltage	HIGH or LOW state	0	V _{CC}	V
		3-state	0	5.5	V
T _{amb}	operating ambient temperature	in free air	-40	+125	°C
t _r , t _f	input rise and fall times	V _{CC} = 1.2 to 2.7 V	0	20	ns/V
		V _{CC} = 2.7 to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input diode current	V _I < 0	-	-50	mA
V _I	input voltage	note 1	-0.5	+6.5	V
I _{OK}	output diode current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage	HIGH or LOW state; note 1	-0.5	V _{CC} + 0.5	V
		3-state; note 1	-0.5	+6.5	V
I _O	output source or sink current	V _O = 0 to V _{CC}	-	±50	mA
I _{CC} , I _{GND}	V _{CC} or GND current		-	±100	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	power dissipation	T _{amb} = -40 to +125 °C; note 2	-	500	mW

Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	-	-	V
			2.7 to 3.6	2.0	-	-	V
V _{IL}	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 µA	2.7 to 3.6	V _{CC} - 0.2	-	-	V
		I _O = -12 mA	2.7	V _{CC} - 0.5	-	-	V
		I _O = -18 mA	3.0	V _{CC} - 0.6	-	-	V
		I _O = -24 mA	3.0	V _{CC} - 0.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 µA	2.7 to 3.6	-	-	0.2	V
		I _O = 12 mA	2.7	-	-	0.4	V
		I _O = 24 mA	3.0	-	-	0.55	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	-	±0.1	±5	µA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	-	±0.1	±5	µA
I _{off}	power-off leakage current	V _I or V _O = 5.5 V	0.0	-	±0.1	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	-	0.1	10	µA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.7 to 3.6	-	5	500	µA

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		1.2	V _{CC}	-	-	V
			2.7 to 3.6	2.0	-	-	V
V _{IL}	LOW-level input voltage		1.2	-	-	GND	V
			2.7 to 3.6	-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -100 μA	2.7 to 3.6	V _{CC} - 0.3	-	-	V
		I _O = -12 mA	2.7	V _{CC} - 0.65	-	-	V
		I _O = -18 mA	3.0	V _{CC} - 0.75	-	-	V
		I _O = -24 mA	3.0	V _{CC} - 1.0	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 100 μA	2.7 to 3.6	-	-	0.3	V
		I _O = 12 mA	2.7	-	-	0.6	V
		I _O = 24 mA	3.0	-	-	0.8	V
I _{LI}	input leakage current	V _I = 5.5 V or GND	3.6	-	-	±20	μA
I _{OZ}	3-state output OFF-state current	V _I = V _{IH} or V _{IL} ; V _O = 5.5 V or GND	3.6	-	-	±20	μA
I _{off}	power-off leakage current	V _I or V _O = 5.5 V	0.0	-	-	±20	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	3.6	-	-	40	μA
ΔI _{CC}	additional quiescent supply current per input pin	V _I = V _{CC} - 0.6 V; I _O = 0	2.7 to 3.6	-	-	5000	μA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

Octal D-type transparent latch with 5 V tolerant inputs/outputs; 3-state

74LVC373A

AC CHARACTERISTICSGND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500$ Ω .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay Dn to Qn	see Figs 8 and 12	1.2	–	14	–	ns
			2.7	1.5	3.5	7.8	ns
			3.0 to 3.6	1.5	3.0 ⁽¹⁾	6.8	ns
	propagation delay LE to Qn	see Figs 9 and 12	1.2	–	16	–	ns
			2.7	1.5	3.4	8.2	ns
			3.0 to 3.6	1.5	3.1 ⁽¹⁾	7.2	ns
t _{PZH} /t _{PZL}	3-state output enable time OE to Qn	see Figs 10 and 12	1.2	–	17	–	ns
			2.7	1.5	4.2	8.7	ns
			3.0 to 3.6	1.5	3.4 ⁽¹⁾	7.7	ns
t _{PHZ} /t _{PLZ}	3-state output disable time OE to Qn	see Figs 10 and 12	1.2	–	8.0	–	ns
			2.7	1.5	3.3	7.1	ns
			3.0 to 3.6	1.5	2.9 ⁽¹⁾	6.1	ns
t _W	LE pulse width HIGH	see Fig.9	2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	1.5 ⁽¹⁾	–	ns
t _{su}	set-up time Dn to LE	see Fig.11	2.7	2.0	–	–	ns
			3.0 to 3.6	2.0	0 ⁽¹⁾	–	ns
t _h	hold time Dn to LE	see Fig.11	2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	0.3 ⁽¹⁾	–	ns
t _{sk(0)}	skew	note 2	–	–	–	1.0	ns

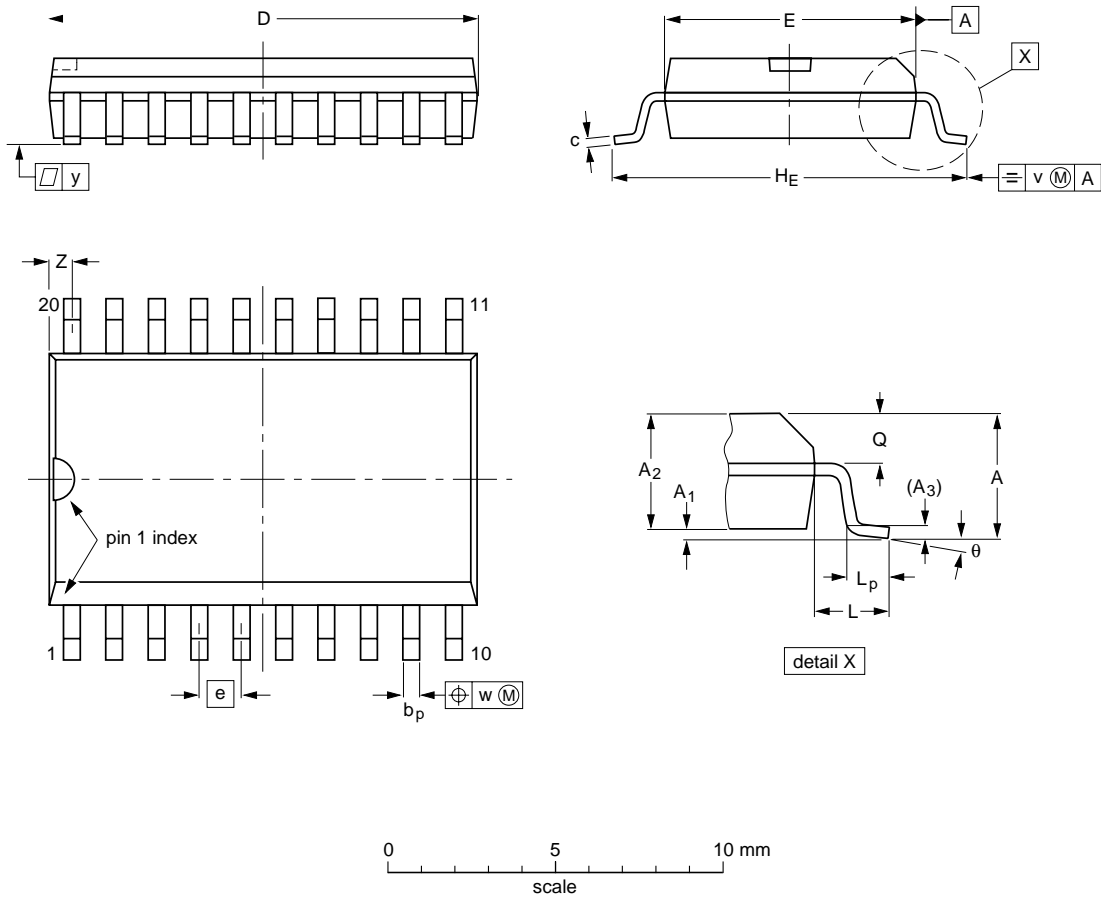
Octal D-type transparent latch with
5 V tolerant inputs/outputs; 3-state

74LVC373A

PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

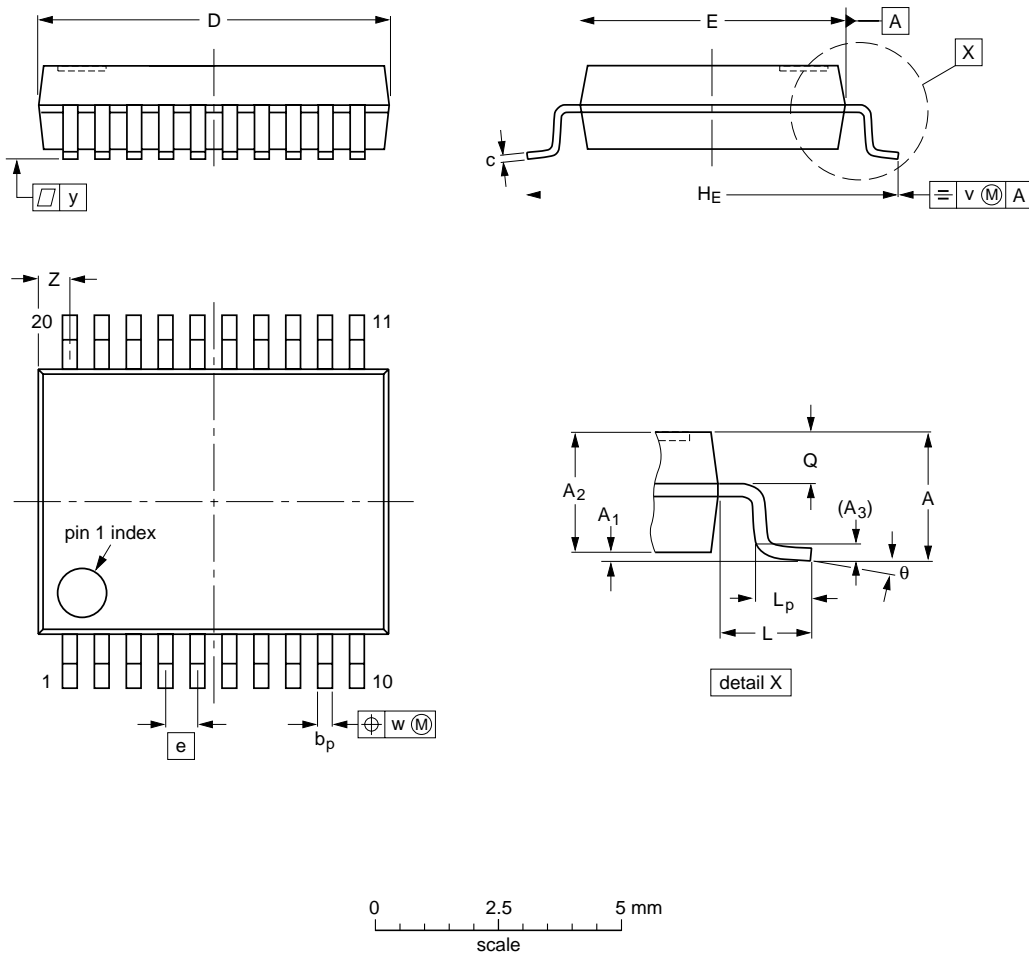
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION
	IEC	JEDEC	JEITA		
SOT163-1	075E04	MS-013			

Octal D-type transparent latch with
5 V tolerant inputs/outputs; 3-state

74LVC373A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION
	IEC	JEDEC	JEITA		
SOT339-1		MO-150			